REMARKS

The Final Office Action mailed May 12, 2003, has been received and reviewed. Claims 19, 21-23 and 25-34 are currently pending in the application. Claims 19, 21-23 and 25-34 stand rejected. Applicant proposes to amend claim 19 and respectfully requests reconsideration of the application as proposed to be amended herein.

Objection to Claim 19

The Examiner objects to claim 19 stating that the phrase ". . . at least one active face-up stack die **one** the layer of conductive epoxy adhesive . . ." should be changed to active face-up stack die *on* the layer of conductive epoxy adhesive. Applicant proposes to amend claim 19 herein accordingly.

35 U.S.C. § 112 Claim Rejections

Claim 19 stands rejected under 35 U.S.C. § 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. Applicant respectfully traverses this rejection, as hereinafter set forth.

The Examiner states that "[e]lectrically connecting said at least one stack die directly to at least one of said conductors is new subject matter." (Office Action, page 3). The Examiner further asks how the stack die directly connects to at least one of the conductors citing the specification and drawings as disclosing the stack die being connected to the adhesive layer 28 and the lower chip 14 and wherein the chip 14 being directly connected to the conductors 20.

Although Applicant maintains that there is adequate support in the specification and drawings for the limitation of "*electrically* connecting said at least one stack die directly to at least one of said conductors," Applicant proposes to amend claim 19 to remove any perceived ambiguity. More specifically, Applicant proposes to amend claim 19 to recite *providing a direct electrical path between said at least one stack die and at least one of said plurality of conductors*. Applicant submits that such is amply supported by the as-filed specification and

drawings to satisfy the requirements of 35 U.S.C. § 112, first paragraph. For example, with reference to FIG. 1, the upper die 12 is electrically coupled to the substrate 16 by means of wires 38, bond pads 36, and terminals 40. (See also, as-filed specification, page 9, lines 6-9). Such a configuration clearly provides ample support for providing a direct electrical path between the upper die and a conductor ("terminal") of the substrate.

Applicant, therefore, submits that claim 19, as proposed to be amended herein, satisfies the requirements of 35 U.S.C. § 112, first paragraph, and respectfully requests reconsideration and allowance thereof.

35 U.S.C. § 103(a) Obviousness Rejections

Obviousness Rejection Based on Japanese Patent No. 5-13665 to Yamauchi in view of U.S. Patent No. 4,377,619 to Schonhorn et al.

Claim 19 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Yamauchi (Japanese Patent No. 5-13665) in view of Schonhorn et al. (U.S. Patent No. 4,377,619). Applicant respectfully traverses this rejection, as hereinafter set forth.

M.P.E.P. 706.02(j) sets forth the standard for a Section 103(a) rejection:

> To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or combine reference teachings. Second, there must be a reasonable expectation of success. Finally, **the prior art reference (or references when combined) must teach or suggest all the claim limitations.** The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991). (Emphasis added).

The 35 U.S.C. § 103(a) obviousness rejection of claim 19 is improper because there is a lack of motivation to combine the references as cited by the Examiner and because the references relied upon by the Examiner fail to teach or suggest the presently claimed invention.

As proposed to be amended herein, claim 19 discloses a method for fabricating a multi-die assembly comprising: providing a substrate including a plurality of conductors; attaching at least one active face-down base die to said substrate in electrical communication with at least

some of said plurality of conductors; *providing a layer of conductive epoxy adhesive to a back side of the at least one base die; placing a back side of at least one active face-up stack die on the layer of conductive epoxy adhesive*; curing the layer of conductive epoxy adhesive and securing the back side of at least one stack die to said at least one base die; providing a direct electrical path between said at least one stack die and at least one of said conductors; and *electrically grounding said at least one base die via said layer of electrically conductive epoxy adhesive and said at least one stack die.*

The Examiner cites Yamauchi as disclosing a multi-die assembly which includes a substrate, an upper and lower die bonded together using epoxy, with the dies being connected to the substrate using wires and conductors. The Examiner states that "Yamauchi fails to disclose the adhesive is [a] conductive epoxy adhesive and curing the layer of conductive epoxy." (Office Action on page 4). The Examiner, then cites Schonhorn as disclosing the formation of a semiconductor device which includes disposing a layer of conductive epoxy adhesive on the substrate, placing a chip on the conductive epoxy adhesive and curing the layer of conductive epoxy adhesive. The Examiner asserts that, in light of Yamauchi and Schonhorn, it would have been obvious to one having ordinary skill in the art, at the time the invention was made, "to modify the device of Yamauchi to prevent metal migration and to secure more firmly the chip to the substrate, as shown by Schonhorn et al." (Office Action, page 4). Applicant respectfully disagrees.

Applicant respectfully submits that Yamauchi and Schonhorn fail to teach or suggest all of the limitations of claim 19 and, further, that there is a lack of motivation to combine Yamauchi and Schonhorn in the manner suggested by the Examiner in order to arrive at Applicant's presently claimed invention.

Yamauchi discloses a method of fabricating a multi-die assembly with at least two TAB chips "joined with an adhesive 7 with end faces having no bump 3 faced (sic) each other." (Constitution). The bumps of the lower TAB chip are joined with solder to a printed board, and the bumps of the upper TAB chip are connected with wire leads which are joined to a pad of the printed board. As noted by the Examiner, Yamauchi fails to teach or suggest that the adhesive used to join the two TAB chips includes a layer of electrically conductive epoxy. Furthermore,

Yamauchi fails to teach or suggest *electrically grounding at least one base die via the adhesive and at least one stack die.*

Schonhorn teaches a method for preventing the spreading of a liquid on a solid surface (such as an adhesive placed on a substrate), as well as the prevention of metal migration (such as silver migration) between conductors deposited on a surface of the substrate. (See, *e.g.*, abstract, col. 3, lines 9-55). However, while Schonhorn discloses the use of a conductive epoxy disposed between a chip and a substrate, it clearly fails to teach or suggest disposing a layer of such conductive epoxy adhesive *to a back side of the at least one base die* and then *placing a back side of at least one active face-up stack die on the layer of conductive epoxy adhesive.* In other words, Schonhorn fails to teach or suggest the use of conductive epoxy adhesive for coupling two *die* together in the manner set forth in claim 19 of the presently claimed invention. Additionally, Schonhorn clearly fails to teach or suggest *electrically grounding said at least one base die via said layer of electrically conductive epoxy adhesive and said at least one stack die.*

Moreover, Applicant submits that there is a lack of motivation to combine Schonhorn with Yamauchi in the manner suggested by the Examiner. Yamauchi does not appear to teach or suggest any electrical interconnection between the two TAB chips. Rather, as discussed above, the bumps of the lower TAB chip are joined with solder to a printed board, and the bumps of the upper TAB chip are connected with wire leads which are joined to a pad of the printed board. Applicant finds no mention of an electrical interconnection between the two TAB chips. Thus, one of ordinary skill in the art would not be motivated to dispose and electrically conductive epoxy adhesive between the two TAB chips as it is apparent that Yamauchi does not seek to form a electrical path therebetween.

Additionally, since no conductors appear to be present between the two TAB chips, Applicant submits that there would be no reason to prevent metal migration therebetween as suggested by the Examiner.

Applicant, therefore, submits that claim 19 is allowable over Yamauchi and Schonhorn, either considered individually or in combination, and respectfully request reconsideration and allowance thereof.

Obviousness Rejection Based on Japanese Patent No. 5-13665 to Yamauchi in view of U.S. Patent No. 4,377,619 to Schonhorn et al. and further in view of U.S. Patent No. 5,323,060 to Fogal et al.

Claims 21-23, 25-29 and 33-34 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Yamauchi (Japanese Patent No. 5-13665) in view of Schonhorn et al.(U.S. Patent No. 4,377,619) and further in view of Fogal et al. (U.S. Patent No. 5,323,060). Applicant respectfully traverses this rejection, as hereinafter set forth.

Applicant notes that claims 21-23, 25-29 and 33-34 are each dependent from claim 19 either directly or by way of intervening claims. As set forth above, Yamauchi and Schonhorn fail to teach or suggest *providing a layer of conductive epoxy adhesive to a back side of the at least one base die*; *placing a back side of at least one active face-up stack die on the layer of conductive epoxy adhesive*; and *electrically grounding said at least one base die via said layer of electrically conductive epoxy adhesive and said at least one stack die.* Additionally, as set forth above, there is a lack of motivation to combine Yamauchi with Schonhorn in the manner suggested by the Examiner.

Applicant further submits that Fogal fails to teach or suggest the subject matter of *providing a layer of conductive epoxy adhesive to a back side of the at least one base die*; *placing a back side of at least one active face-up stack die on the layer of conductive epoxy adhesive*; and *electrically grounding said at least one base die via said layer of electrically conductive epoxy adhesive and said at least one stack* die.

Indeed, Applicant submits that Fogal teaches away from claim 19 of the presently claimed invention in that Fogal expressly teaches that the "[a]dhesive 38 preferably comprises an electrically *insulating* material" (col. 3, lines 8-9, emphasis added). Applicant, therefore, submits that the teachings of Fogal and the teachings of Schonhorn are incompatible inasmuch as Schonhorn teaches the use of an electrically *conductive* adhesive and Fogal teaches the use of an electrical *insulating* adhesive.

Applicant further submits that there is a lack of motivation to combine the teachings of Fogal with those of Yamauchi. More particularly, Yamauchi teaches back-to-back arrangements of the semiconductor dies while Fogal teaches face-to-back arrangements of semiconductor die

with no apparent suggestion in either of such references that the teachings of one are applicable to the other.

Applicant, therefore, submits that claims 21-23, 25-29, 33 and 34 are allowable over Yamauchi, Schonhorn, and Fogal, either considered individually or in combination, and respectfully requests reconsideration and allowance of the same.

Obviousness Rejection Based on Japanese Patent No. 5-13665 to Yamauchi in view of U.S. Patent No. 4,377,619 to Schonhorn et al. and U.S. Patent No. 5,323,060 to Fogal et al. and further in view of U.S. Patent No. 5,399,898 to Rostoker

Claims 30-32 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Yamauchi (Japanese Patent No. 5-13665) in view of Schonhorn et al.(U.S. Patent No. 4,377,619) and Fogal et al. (U.S. Patent No. 5,323,060) and further in view of Rostoker (U.S. Patent No. 5,399,898). Applicant respectfully traverses this rejection, as hereinafter set forth.

Each of claims 30-32 depend from claim 19 either directly or through intervening claims. As set forth above, Yamauchi, Schonhorn and Fogal clearly fail to teach or suggest all of the subject matter of the presently claimed invention as set forth in independent claim 19. Particularly, Yamauchi, Schonhorn and Fogal fail to teach or suggest providing a layer of electrically conductive adhesive and grounding the base stack die through the layer of conductive epoxy adhesive. Applicant further submits that Rostoker fails to teach or suggest such subject matter.

Additionally, Applicant submits that there is a lack of motivation to combine the teachings of the references relied upon by the Examiner. As noted above, there is a lack of motivation to provide the conductive adhesive of Schonhorn between the two TAB chips of Yamauchi since Yamauchi fails to teach or suggest that any electrical connection is desirable between the stacked TAB chips. Furthermore, as noted above, there is a lack of motivation to combine Fogal with Schonhorn since Fogal teaches the use of electrically *insulating* adhesive while Schonhorn teaches the use of electrically *conductive* adhesive. Additionally, Yamauchi teaches back-to-back arrangements of the semiconductor dies while Rostoker teaches face-to-

face arrangements of semiconductor die with no apparent suggestion in any of the references that the teachings of one are applicable to the other.

Moreover, with respect to claims 31 and 32, while the Examiner points to FIG. 4A of Rostoker as teaching the subject matter of bridging two base die with a stack die, Applicant submits that one of ordinary skill in the art would lack motivation to combine such a teaching with Yamauchi. Rostoker explicitly states that such an embodiment requires increased substrate surface area (see, e.g., col. 15, lines 9-11) thereby teaching away from Yamauchi which states that its disclosed arrangement is desirable because it substantially *reduces* mounting area.

Applicant, therefore, submits that claims 30-32 are allowable over Yamauchi, Schonhorn, Fogal and Rostoker, either considered individually or in combination, and respectfully requests reconsideration and allowance of the same.

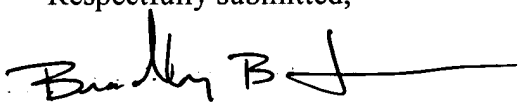
ENTRY OF AMENDMENTS

The proposed amendments to claim 19 above should be entered by the Examiner because the amendments are supported by the as-filed specification and drawings and do not add any new matter to the application. Further, Applicant submits that the amendments do not raise new issues or require a further search. Finally, if the Examiner determines that the amendments do not place the application in condition for allowance, entry is respectfully requested upon filing of a Notice of Appeal herein.

CONCLUSION

Claims 19, 21-23 and 25-34 are believed to be in condition for allowance, and an early notice thereof is respectfully solicited. Should the Examiner determine that additional issues remain which might be resolved by a telephone conference, he is respectfully invited to contact Applicant's undersigned attorney.

Respectfully submitted,



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